FPG-EYE

A modular Lattice XP2 FPGA platform with a CMOS Camera

Introduction

FPG-EYE is a powerful prototyping board that allows you to implement complex applications by using the Mico32 softcore and the flexibility of the FPGA logic.

The board includes external RAM and Flash memories to store big amount of data, and it also includes Ethernet, serial, and 802.15.4 radio for wired and wireless connections.

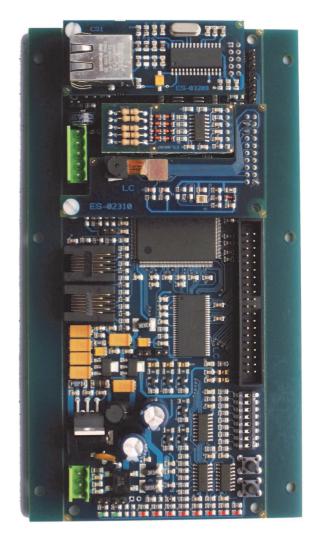
The onboard CMOS camera coupled with the FPGA flexibility allows you to run vision algorithms in real time, and to mix hardware and software implementations.

Hardware description

- FPGA Lattice LFXP2-17E-5QN208C, with 17k LUT.
 The FPGA hosts a complete system-on-a-chip powered by a 50 MHz Lattice Mico32 softcore and all the peripheral controllers, or a design of your choice;
- 512 kB 16 bit 12 ns SRAM, for code and data;
- 32 MB 16 bit 133 MHz SDRAM, used for storing CMOS camera images and data;
- 2 MB Serial Flash, used for storing code and persistent data to be loaded into the SRAM at boot time;
- High Efficiency Switching power supply LM2575, which accepts 5-28V AC or 7-40V DC;
- 2 RJ45 connectors, 12 LEDs, 8 switches, 2 button, 1 real-time clock, MOSFET switches to power-off peripherals, and 3rd-party plugin / Display connector;
- 72mm DIN bar size, also compatible with TEKO plastic cases "TK series" (e.g., TK22, TK33, TK44).

Four plugin boards are also available:

- Ethernet Plugin Board¹
 up to 10 Mb/s using an SPI ENC28J60 controller.
- Radio Board¹
 with a Microchip MRF24J40MB 802.15.4 Transceiver.
- Serial Board with RS232-TTL voltage conversion.
- Camera Board providing a color CMOS Camera (HV7131GP), with 640x480 resolution at 30 fps, plus a light sensor.



FPG-EYE board hosting Ethernet, Serial, and Camera plugin boards.



¹ Ethernet and Radio plugin boards are mutually exclusive.

Software

The FPG-EYE platform is provided with a **rich set of software components**.

The development environment is based on the Lattice Mico32 development environment.



FPG-EYE is provided with **ERIKA Enterprise**, an **open-source real-time operating system** implementing the OSEK/VDX API.

http://erika.tuxfamily.org

A set of **libraries** are already integrated in the build environment:

- TCP/IP stack using the LWIP library;
- 802.15.4 radio stack using the uWireless library;
- CMOS Camera;
- · UART and console drivers;
- · Light sensor;
- Buttons, LEDs, switches.

FPG-EYE comes with a set of **demo applications**:

- web server with CMOS camera image acquisition;
- serial console;
- 802.15.4 uWireless stack.

Finally, FPG-EYE supports the **CAL Language** to provide HW/SW partition of **dataflow applications** on Verilog blocks and C functions. The CAL Language support has been developed under the IST FP7 ACTORS Project.

http://www.actors-project.eu

Pre-built FPGA configurations

To allow a quick startup, the FPG-EYE platform is provided with a set of **pre-built FPGA configurations** including:

- the Mico32 softcore;
- · Wishbone bus:
- CMOS Camera peripheral a DMA-enabled wishbone peripheral that controls the CMOS camera, to implement simple vision applications;
- SRAM, SDRAM, Serial Flash controllers;
- UART, SPI and I2C peripherals;
- Ethernet or 802.15.4 support.

The all-inclusive FPGA configuration uses around 8k LUTs.

Thanks to these pre-built images, it is possible to start developing new peripherals in a few minutes!

Custom designs are also possible in Verilog and VHDL, using Lattice tools.

How to buy the FPG-EYE board

The FPG-EYE board is available from Evidence Srl and from selected distributors.

For orders and additional information, please visit the web site:

http://www.evidence.eu.com

or contact us by writing an e-mail to:

info@evidence.eu.com

Evidence SRL, established in 2002, is a spin-off company of the ReTiS Lab of the Scuola Superiore S. Anna, Pisa-Italy. We are experts in the domain of embedded and real-time systems with profound knowledge of the design and specification of embedded software. We keep providing significant advances in the state of the art of real-time analysis, multicore scheduling and much more.

