135 ORIG

005120

4877 ATM.

Features

- Paged Configurations with Page Reset on Power-Up
  - AT27C512 – Not Paged, 64K x 8
  - AT27C513 – 4 Pages, 16K x 8
  - AT27C515 – 2 Pages, 32K x 8
- Low Power CMOS Operation
  - 40mA max. Active at 5MHz
  - 100µA max. Standby
- Fast Read Access Time – 120ns
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Two-Line Control & JEDEC Standard Pinout
- CMOS & TTL Compatible
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

512K CMOS

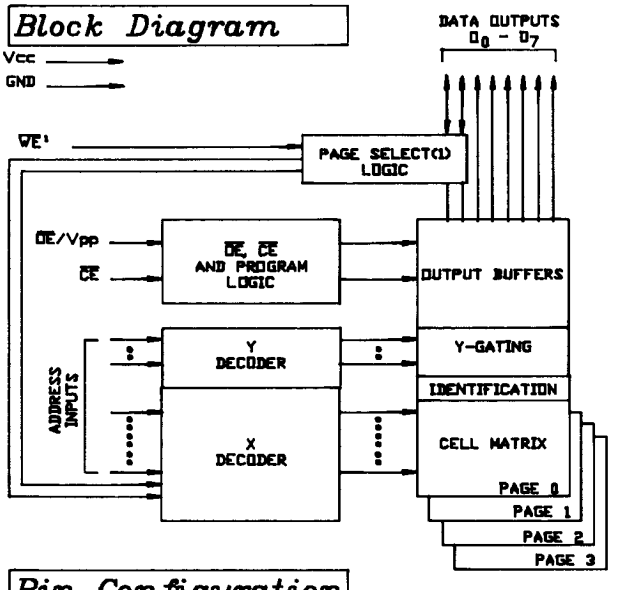
UV ERASABLE

PROM

247776

AT27C512
AT27C513
AT27C515

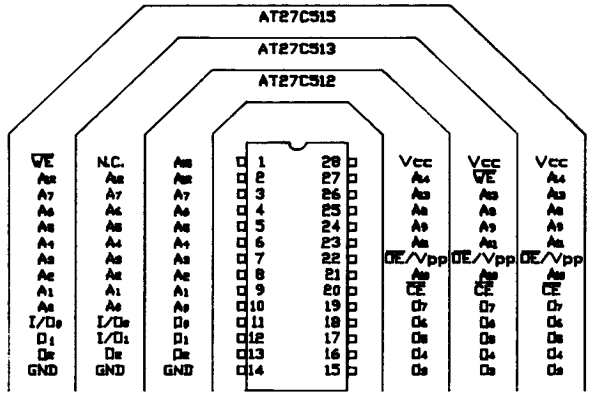
Block Diagram



Part	Address Pins	Number of Pages (1)	Bits Per Page
AT27C512	$A_0 - A_{15}$	–	524,288
AT27C513	$A_0 - A_{15}$	4	131,072
AT27C515	$A_0 - A_{14}$	2	262,144

(1) AT27C513 and AT27C515 only

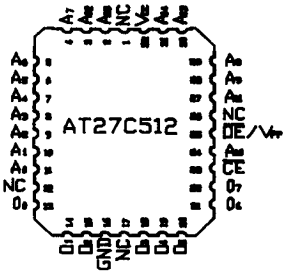
Pin Configuration



Note: Pin 1 (N.C.) on AT27C513 can be left floating or tied to any voltage between -0.1V and Vcc + 1V

PIN NAMES

$A_0 - A_{15}$	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/V_{PP}
$\overline{VE}$	PAGE WRITE ENABLE
I/O_0-I/O_8	INPUT/OUTPUT
O_0-O_7	OUTPUTS
N.C.	NO CONNECT



Description

The ATMEL 27C512, 27C513, 27C515 is a family of low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memories (EPROM). These devices require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

The AT27C512 is organized 64K x 8. The AT27C513 and AT27C515 feature page mode addressing. ATMEL's 27C513 has 4 pages, each organized 16K x 8, and provides a compatible upgrade for existing 128K EPROM based designs. The AT27C515 presents 2 pages of 32K x 8 memory to allow a doubling of available memory in existing systems using 256K EPROM. Both increased memory capacity and improved system performance can now be easily retrofitted without using costly additional board space.

The AT27C513 and AT27C515 have an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latches are automatically reset to page 0 upon power-up (resets typically for V_{cc} < 3.8V).

ATMEL's 1.5 micron CMOS technology provides optimum speed, low power and high noise immunity. Power consumption is typically only 15mA in Active Mode and less than 10uA in Standby. In addition to the speed, power and reliability advantages of the CMOS process, the CMOS technology is an extension of ATMEL's high quality and highly manufacturable floating poly EPROM technology.

These parts are available in industry standard JEDEC-approved 28-pin DIP or 32-pad LCC packages. All devices feature a two line control ($\overline{CE}$,$\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a high density 64K byte storage capability, the ATMEL 512K EPROMs allow firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

All ATMEL 512K EPROMs have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. Programming time is typically 4 msec per byte. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Operating Modes

PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	AI	V_{CC}	Outputs	I^3/O_I
MODE	(20)	(22)			(28)	(13,15-19)	(11,12)
Read	V_{IL}	V_{IL}	V_{IH}	AI	V_{CC}	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X[1]	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z	High Z
Fast PGM[2]	V_{IL}	V_{PP}	V_{IH}	AI	V_{CC}	D_{IN}	D_{IN}
PGM Inhibit	V_{IH}	V_{PP}	V_{IH}	X	V_{CC}	High Z	High Z
Page Select Write[3]	V_{IL}	V_{IH}	V_{IL}	X	V_{CC}	High Z	Page D_{IN}
Product Identification	V_{IL}	V_{IL}	V_{IH}	[4,5]	V_{CC}	Ident.Code	Ident.Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to programming characteristics.
3. AT27C513 and AT27C515 only.
4. V_H = 12.0±0.5V.
5. Two identifier bytes may be selected. All AI inputs are held low (V_{IL}), except A_9 which is set to V_H and A_0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Page Selection Data (27C513 & 27C515 Only)

Part	27C513		27C515
Input/Output Pin	I/O_1	I/O_0	I/O_0
Page Selection	[12]	[11]	[11]
Select Page 0	V_{IL}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}	V_{IH}
Select Page 2	V_{IH}	V_{IL}	-
Select Page 3	V_{IH}	V_{IH}	-

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) w/Respect to Ground	-0.6V to +6.25V
All Output Voltages w/Respect to Ground	-0.6V to V_{CC}+0.6V
Voltage on Pin 24 w/Respect to Ground	-0.6V to +13.5V
V_{PP} Supply Voltage w/Respect to Ground	-0.6V to +14.0V
Integrated UV Erase Dose	7258 W*sec/cm^2

*NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Conditions for Read and Page Select Operation

		27C512-12 27C513-12 27C515-12	27C512-15 27C513-15 27C515-15	27C512-17 27C513-17 27C515-17	27C512-20 27C513-20 27C515-20	27C512-25 27C513-25 27C515-25
Operating Temperature	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.[2]		-40°C- 85°C	-40°C- 85°C	-40°C- 85°C	-40°C- 85°C
	Mil.[2]		-55°C- 125°C	-55°C- 125°C	-55°C- 125°C	-55°C- 125°C
V_{CC} Power Supply[1]		5V± 5%	5V±10%	5V±10%	5V±10%	5V±10%

D.C. and Operating Characteristics for Read and Page Select Operation

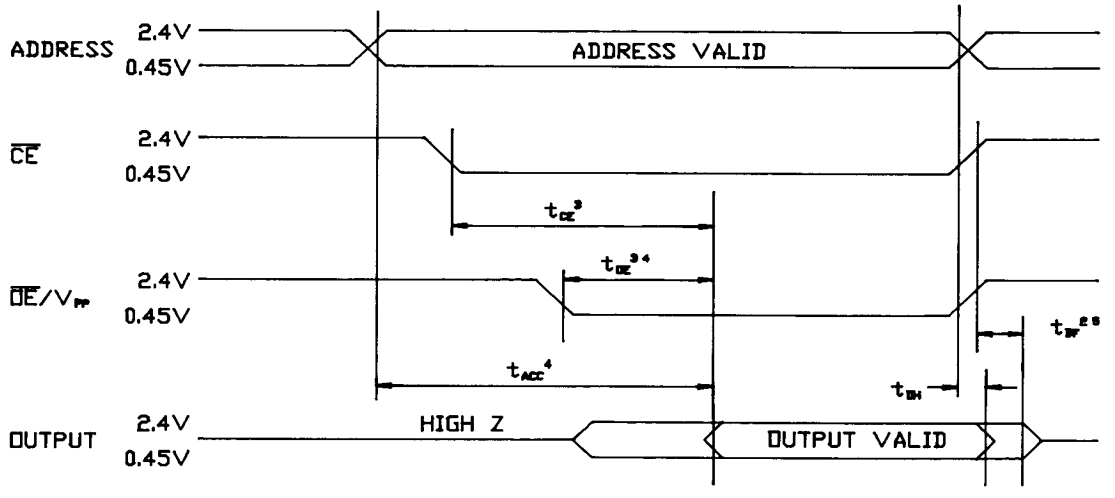
Symbol	Parameter		Min	Max	Units	Test Conditions
I_{LI}	Input Load Current			10	uA	V_{IN}=-0.1 to V_{CC}+1.0V
I_{LO}	Output Leakage Current			10	uA	V_{OUT}=-0.1 to V_{CC}+0.1V
I_{SB}	V_{CC} Standby Current	Com.		100	uA	$\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V
		Ind.,Mil.		200	uA	
		Com.		2	mA	$\overline{CE}$=2.0 to V_{CC}+1.0V
		Ind.,Mil.		3	mA	
I_{CC}	V_{CC} Active Current	Com.		40	mA	f=5MHz, $\overline{CE}$=V_{IL}, I_{OUT}=0mA
		Ind.,Mil.		50	mA	
V_{IL}	Input Low Voltage		-.1	+0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=2.1mA
V_{OH}	Output High Voltage		2.4		V	I_{OH}=-400uA
			V_{CC}-0.1		V	I_{OH}=-50uA

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

A.C. Characteristics for Read Operation

Symbol	Parameter	27C512-12 27C513-12 27C515-12 Min	Max	27C512-15 27C513-15 27C515-15 Min	Max	27C512-17 27C513-17 27C515-17 Min	Max	27C512-20 27C513-20 27C515-20 Min	Max	27C512-25 27C513-25 27C515-25 Min	Max	Units	Test Conditions
t_{ACC}	Address to Output Delay		120		150		170		200		250	ns	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200		250	ns	$\overline{OE}/V_{PP}=V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		65		70		70		75		100	ns	$\overline{CE}=V_{IL}$
t_{DF}[2,5]	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float		50		50		50		55		60	ns	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ whichever occurred first		0		0		0		0		0	ns	$\overline{CE}=\overline{OE}/V_{PP}=V_{IL}$

A.C. Waveforms for Read Operation



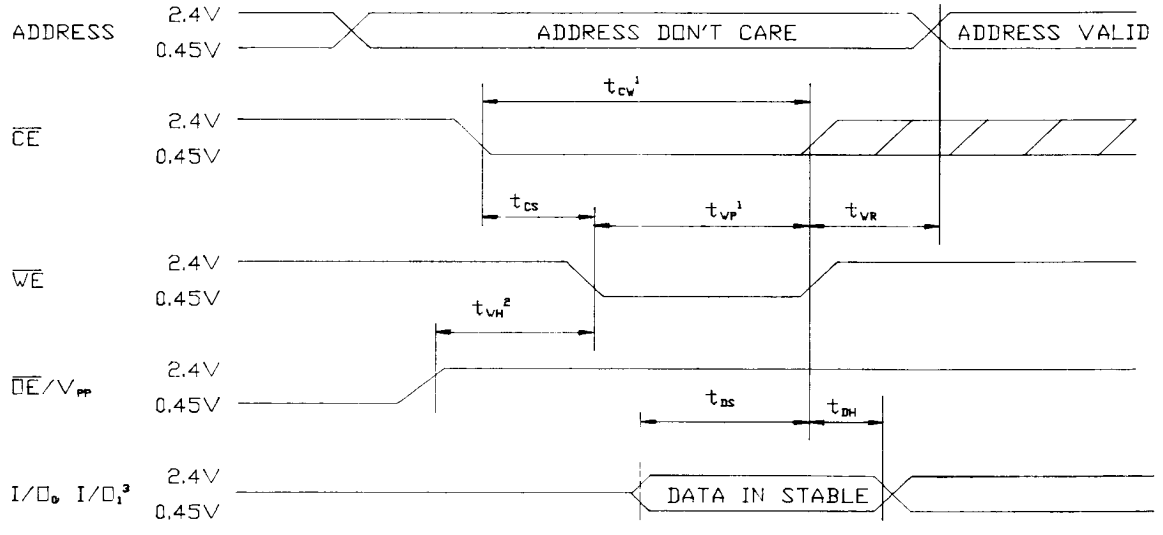
Notes:

1. Timing measurement references are 0.8V and 2.0V. Input Driving Levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

A.C. Characteristics for Page Select (27C513 & 27C515 Only)

Symbol	Parameter	27C513-12 27C515-12 Min	Max	27C513-15 27C515-15 Min	Max	27C513-17 27C515-17 Min	Max	27C513-20 27C515-20 Min	Max	27C513-25 27C515-25 Min	Max	Units	Test Conditions
t_{CV}	$\overline{CE}$ to End of Write		110		110		125		145		180	ns	$\overline{OE}/V_{PP}=V_{IH}$
t_{VP}	Write Pulse Width		60		60		70		80		100	ns	$\overline{OE}/V_{PP}=V_{IH}$
t_{VR}	Write Recovery Time		20		20		20		20		20	ns	
t_{DS}	Data Setup Time		35		35		40		45		50	ns	$\overline{OE}/V_{PP}=V_{IH}$
t_{DH}	Data Hold Time		20		20		20		20		20	ns	$\overline{OE}/V_{PP}=V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time		0		0		0		0		0	ns	$\overline{OE}/V_{PP}=V_{IH}$
t_{VH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time		50		50		50		50		55	ns	

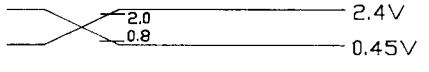
A.C. Waveforms for Page Select (27C513 & 27C515 Only)



Notes:

1. Writing can be terminated by either $\overline{CE}$ or $\overline{WE}$ going high after the minimum t_{VP} requirement has been met.
2. $\overline{OE}/V_{PP}$ must be high during a Page Select Write.
3. Page Select Inputs (I/O_1 is only for 27C513)

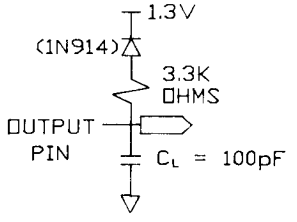
Input Test Waveforms and Measurement Levels



AC MEASUREMENT LEVELS AC DRIVING LEVELS

t_R, t_F 10 to 90% ≤ 20ns

Output Test Load



Note: C_L = 100pF Including jig capacitance.

Pin Capacitance

(f = 1MHz T = 25°C)

	TYP[1]	MAX	UNITS	CONDITIONS
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltages.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{OE}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions (see note 1)
I_{LI}	Input Current (All Inputs)		10	µA	$V_{IN}=V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}+1	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL}=2.1mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH}=-400µA
I_{CCE}	V_{CC} Supply Current (Program & Verify)		40	mA	
I_{PPE}	$\overline{OE}/V_{PP}$ Supply Current (Program)		25	mA	$\overline{CE}=V_{IL}$
V_{ID}	A_9 Product Identification Voltage	11.5	12.5	V	

Notes:
1. Vcc must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.
3. Initial Program Pulse width tolerance is 1 msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

A.C. Programming Characteristics

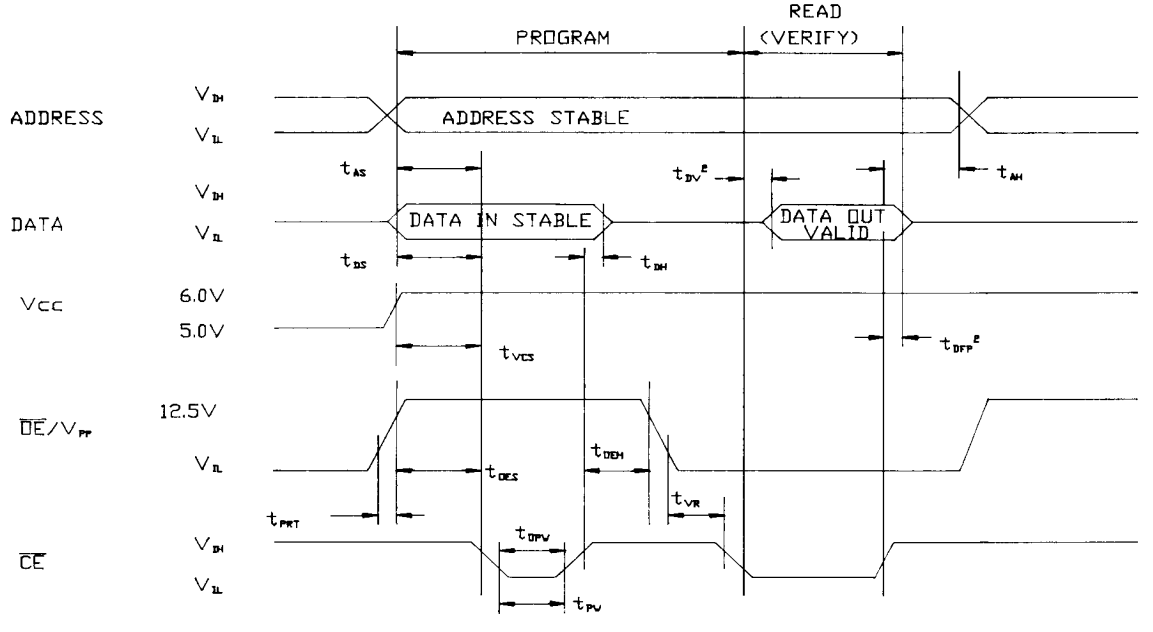
T_A=25±5°C, V_{CC}=6.0±0.25V, $\overline{OE}/V_{PP}$=12.5±0.5V

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit
t_{AS}	Address Setup Time	2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DFP}[2]	$\overline{CE}$ High to Output Float Delay	0		130	ns
t_{VCS}	V_{CC} Setup Time	2			µs
t_{PW}[3]	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[4]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{DV}	Data Valid from $\overline{CE}$			1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns

*A.C. Conditions of Test

Input Rise and Fall Times (10% to 90%)	20ns
Input Pulse Levels	0.45V to 2.4V
Input Timing Reference Level	0.8V to 2.0V
Output Timing Reference Level	0.8V to 2.0V

Programming Waveforms[1,3,4]



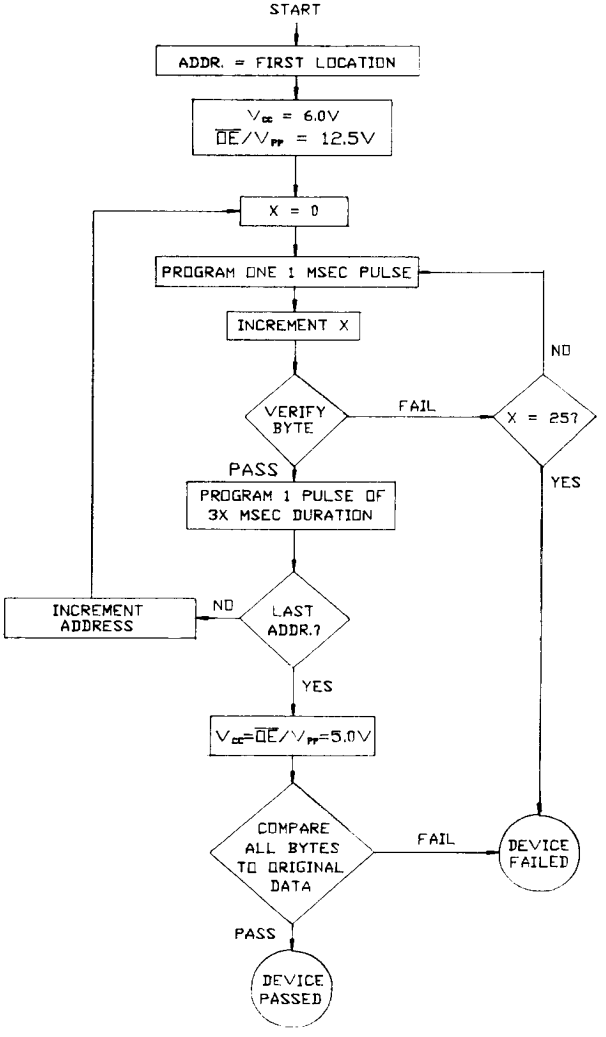
Notes:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page select write operation prior to programming the 27C513 or 27C515.
4. When programming a 27C512/513/515 a 0.1µf high frequency bypass capacitor is required across V_{PP} and ground to suppress noise transients which may prevent proper programming of the part.

Fast Programming Algorithm

Two $\overline{CE}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V and $\overline{OE}/V_{PP}$[1] is raised to 12.5V. The first $\overline{CE}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CE}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the over-program pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max.)

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} and $\overline{OE}/V_{PP}$[1] are lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.



ATMEL's 27C512, AT27C513, and AT27C515 Integrated Product Identification Code

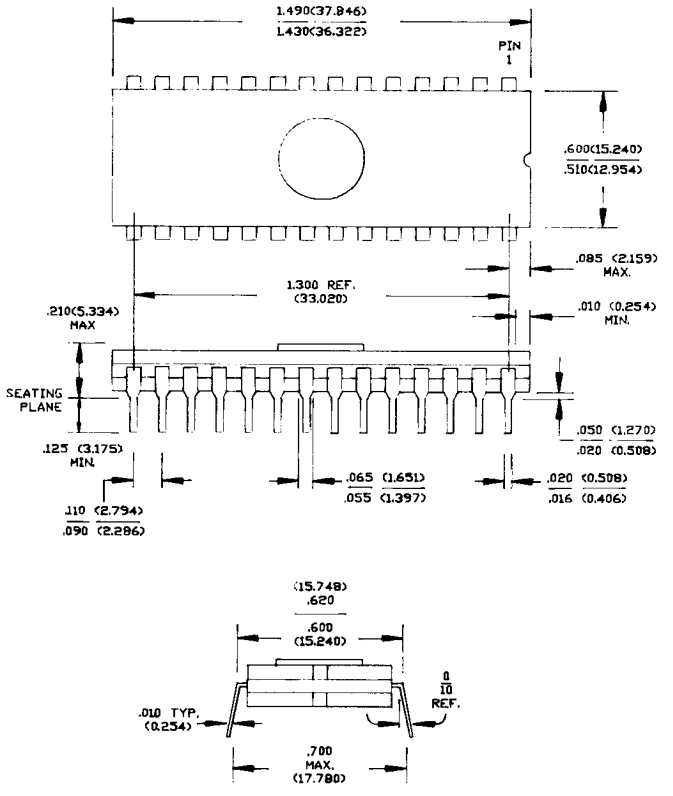
Codes	Pins A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Mfg.	0	0	0	0	1	1	1	1	1	1F
Device Type										
AT27C512	1	0	0	0	0	1	1	0	1	0D
AT27C513	1	0	0	0	0	1	1	1	0	0E
AT27C515	1	1	0	0	0	1	1	1	1	8F

Erasure Characteristics

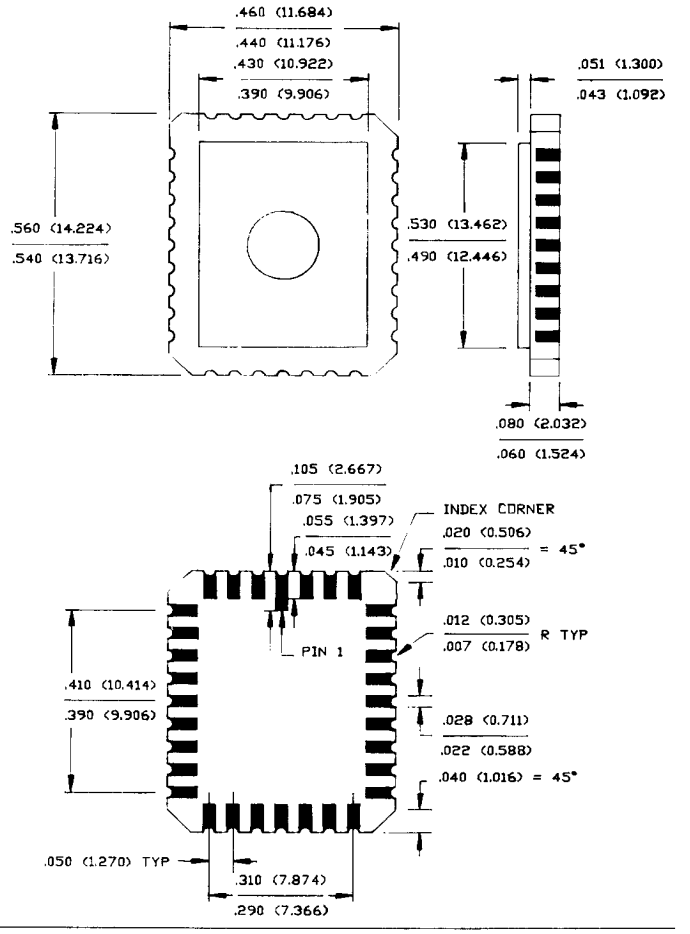
The entire memory array of the AT27C512, AT27C513, or AT27C515 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537A. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000$_u$W/cm^2 intensity lamps spaced one inch away from the AT27C512, AT27C513, or AT27C515. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W*sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Packaging Information

28-Lead Hermetic Dual In-Line CERDIP
Package Type D
DIMENSIONS IN INCHES AND (MILLIMETERS)



32-Pad Ceramic Leadless Chip Carrier Package Type L
DIMENSIONS IN INCHES AND (MILLIMETERS)



Ordering Information

EPROMs + EEPROMs - EXAMPLE: 27C515-15DM1B

PREFIX	DEVICE	SUFFIX
AT	27C512	25 P C 1 B
	27C513	20 D I 2 /883
	27C515	17 L M
		15
		12

PROCESSING
- BLANK = STANDARD PROCESSING
- B = MIL-STD-883, Class B Method 5004 (Non-Compliant)
- /883 = MIL-STD-883, Class B Fully Compliant

POWER SUPPLY
- 2 = 5V±5%
- 1 = 5V±10%

TEMPERATURE RANGE
- C = COMMERCIAL (0°C TO 70°C)
- I = INDUSTRIAL (-40°C TO +85°C)
- M = MILITARY (-55°C TO +125°C)

PACKAGE
- P = PLASTIC
- D = CERDIP
- L = LEADLESS CHIP CARRIER

SPEED

FSCM 1FN41

2095 Ringwood Ave., San Jose, CA 95131 (408) 434-9201

February 1987
ORDER NO. AT27C512 - 0002