BCD Counter

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Abstract

Designing a simple, but human friendly digital counter can present several problems for an engineer to overcome. Here a circuit is created around discrete logic ICs, 7-segment displays and a rotary telephone dial to explore these issues.

1 Introduction

Traditionally digital circuits count in binary, a numbering system foreign to the average person. Egineers are required to create solutions in software or hardware to convert the binary to decimal, or base ten, a system familiar and useful to the everyday person. However, a third option exists: counting in binary coded decimal.

A digital counter was designed using TTL logic chips, a rotary telephone dial as an input and a pair of 7-segment displays for output to tackle this, and few other peripheral digital design issues, for the purpose of hands-on-learning.

2 Design Challenges

In order for the counter to be succesful, the input and output of the system must be accurate and predictable. The counter must count up by the number entered via the rotary telephone dial, and the display should count in decimal, not hexidecimal or binary. This means that when a digit is at 9, the next count should cause it to roll over to zero, and increment the next most significat digit.

2.1 Roll-Your-Own Carry

At the heart of the BCD counter are two 74LS93 4-bit binary counters. The first one counts the "ones" place, and the second countering the "tens" place. The decimal count is displayed on two identical 7-segment LED display which are each driven by a 74LS47 display driver chips.

In order to do this, a truth table is created (see table 1) to define the boolean expresion (see equation 1) to trigger a rollover condition (incrementing from nine to ten).

D	C	B	A	X
0	0	0	0	0
0	0	0	1	0
	...			0
1	0	0	1	0
1	0	1	0	1

Table 1: Greater than nine truth table.

$$X = (BD) \tag{1}$$

The truth table shows us that when monitoring a 4 bit number (ABCD, A is MSD, D is LSD) BCD roll-over and carry happens at a logic level of B AND D. The 74LS93 expects a low logic level to reset (roll-over) on pin R0(2). However, in order to increment the next counter (carry) we need a logic level of high on the next counter's CKA pin. This situation gives us the circuit shown in Figure 1.

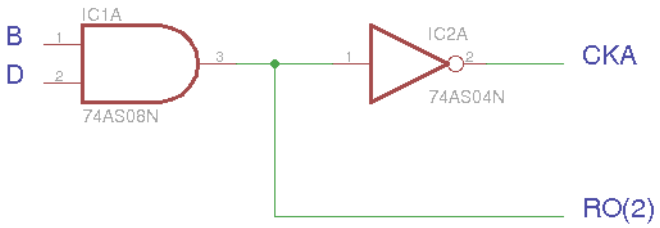

Figure 1: Resulting logic from truth table.

The circuit in Figure 1 requires the use of two different integrated circuits, an AND gate and a hex inverter. Using NAND gates (see figure 2), we can create the same logic with the use of only one IC.

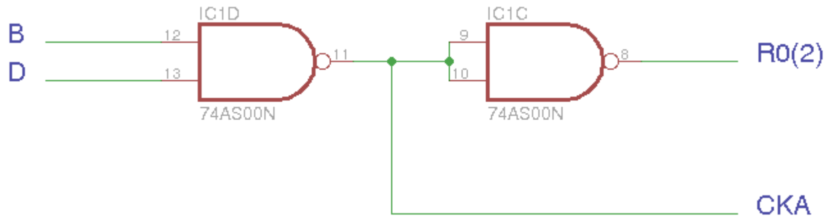

Figure 2: Logic created from NAND gates.

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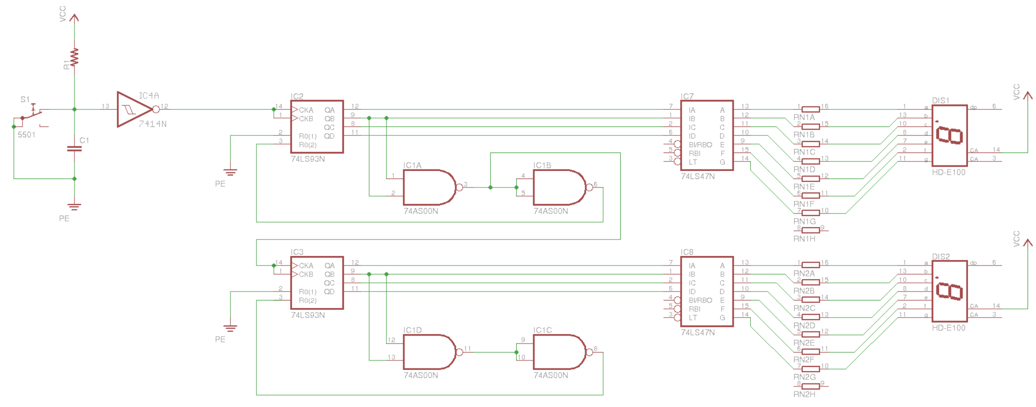

Figure 3: Counter circuit.

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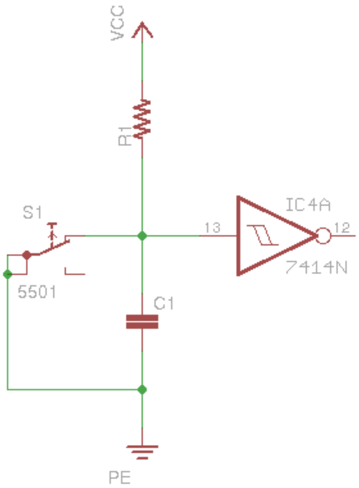

Figure 4: Debounce circuit.

$$V_{pin} = Vcc[1 - e^{(-t/\tau)}] \tag{2}$$

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$$\tau = RC = 10k\Omega(\underbrace{C_1 \parallel C_2}_{20nF}) = 5ms \tag{3}$$